DERWENT-ACC-NO: 2002-729571

DERWENT-WEEK: 200279

TITLE: Stacked chip package

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PATENT-ASSIGNEE: SAMSUNG ELECTRONICS CO LTD[SMSU]

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PATENT-FAMILY:

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APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
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2000KR-0072322			December 1, 2000

INT-CL (IPC): H01L023/28

ABSTRACTED-PUB-NO: KR2002042958A

BASIC-ABSTRACT:

NOVELTY - A stacked chip package is provided to reduce a thickness of the stacked chip package by using a thickness of a substrate.

DETAILED DESCRIPTION - The first and the second chip mounting holes(35,45) are formed in a center portion of an upper portion of a substrate(31) such as a printed circuit board, a ceramic substrate, and a tape-wired substrate. The first mounting hole(35) is larger than the second mounting hole(45). A stepped

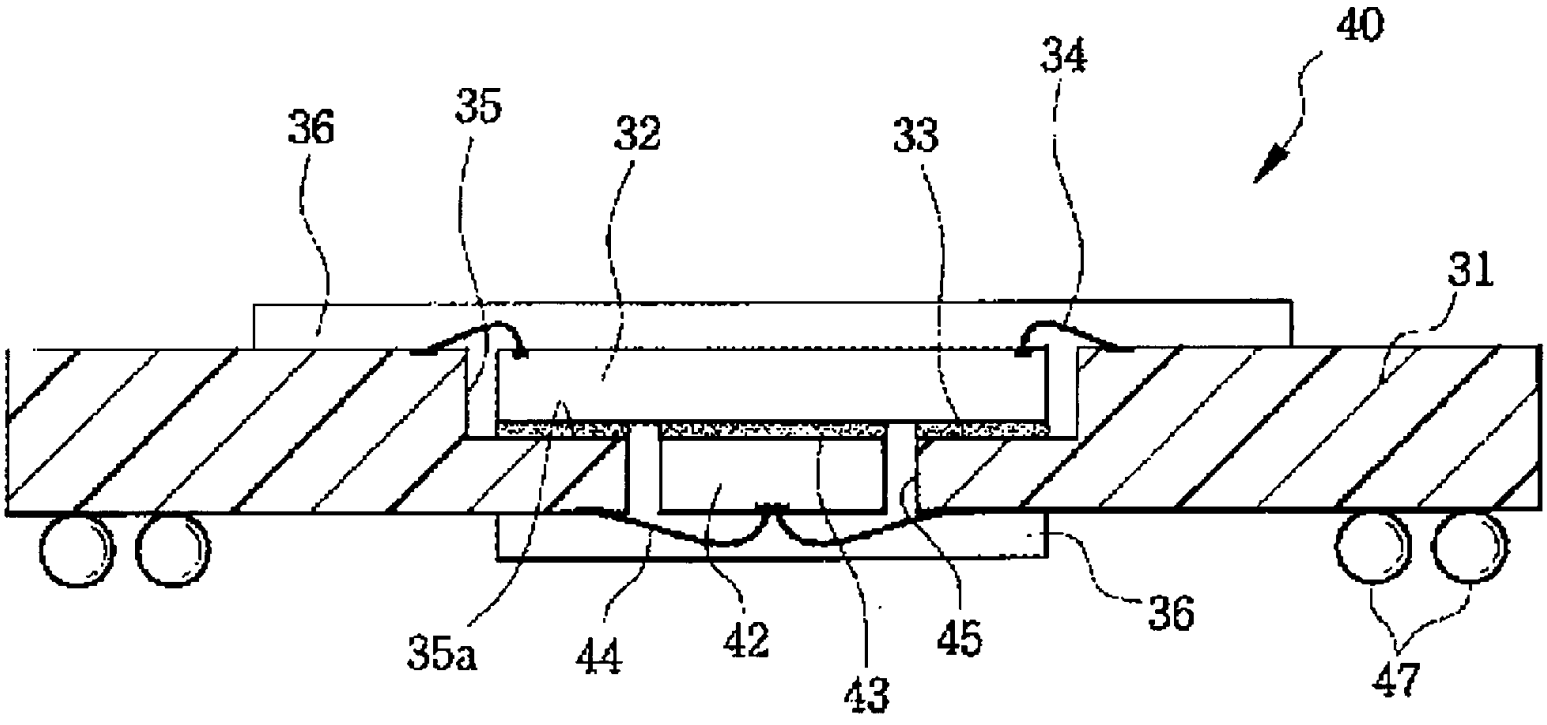
portion(35a) is formed in an inside of the first and the second chip mounting holes(35,45). The first chop(32) is adhered to the stepped portion(35a) through the first chip mounting hole(35) by using an adhesive(33). The first chip(32) is connected with a wiring pattern of the substrate(31) by a bonding wire(34). The second chip(42) is adhered to a lower side of the first chip(32) through the second chip mounting space(45) by using an adhesive(43). The second chip(42) is connected with a wiring pattern of the substrate(31) by a bonding wire(44).

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: STACK CHIP PACKAGE

DERWENT-CLASS: U11

EPI-CODES: U11-E02A1;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